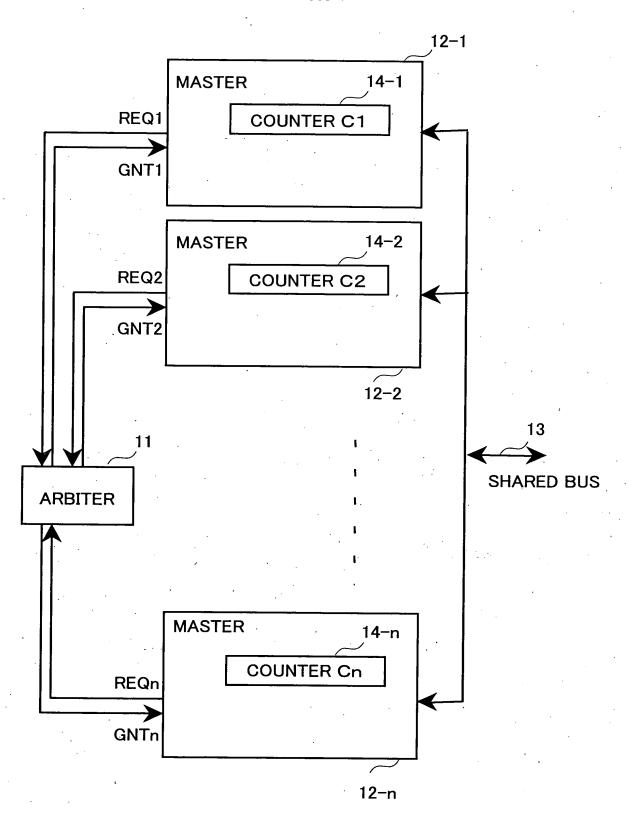
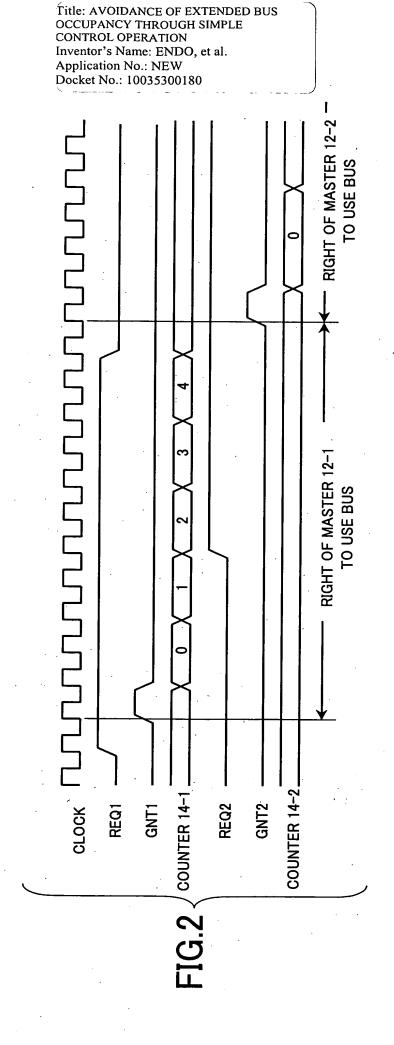
Title: AVOIDANCE OF EXTENDED BUS OCCUPANCY THROUGH SIMPLE

CONTROL OPERATION

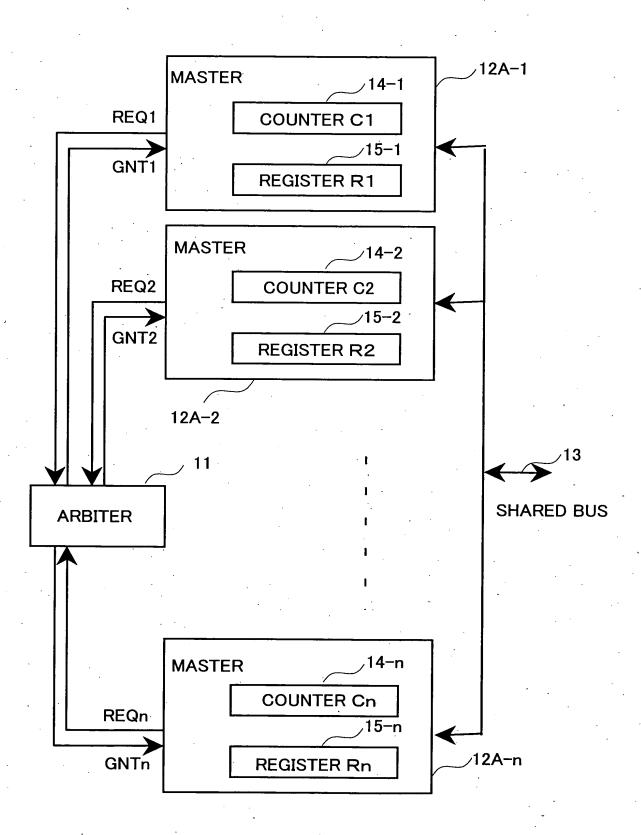
FIG.1





Title: AVOIDANCE OF EXTENDED BUS OCCUPANCY THROUGH SIMPLE CONTROL OPERATION

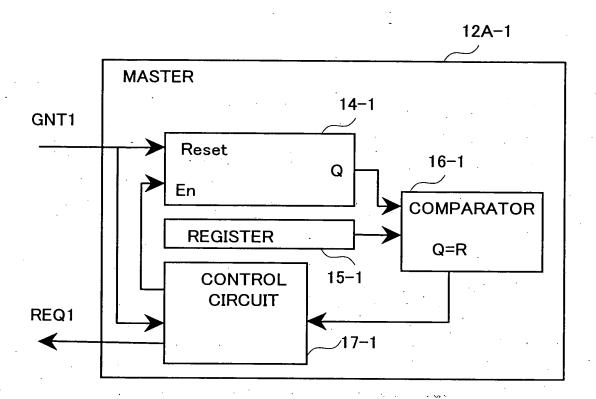
FIG.3



Title: AVOIDANCE OF EXTENDED BUS OCCUPANCY THROUGH SIMPLE CONTROL OPERATION Inventor's Name: ENDO, et al.

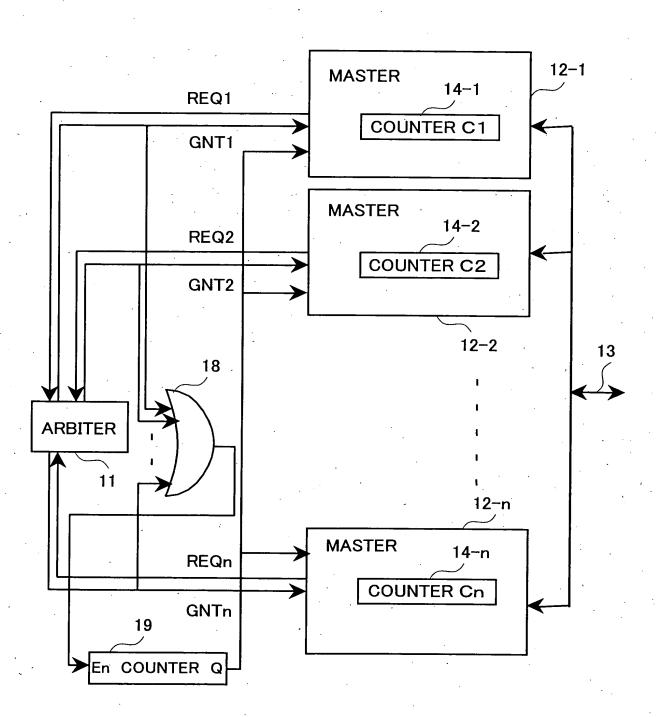
Application No.: NEW Docket No.: 10035300180

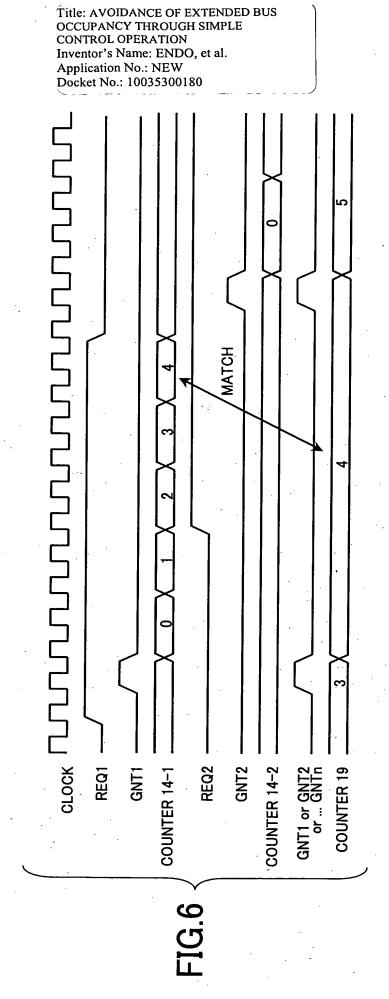
FIG.4



Title: AVOIDANCE OF EXTENDED BUS OCCUPANCY THROUGH SIMPLE CONTROL OPERATION

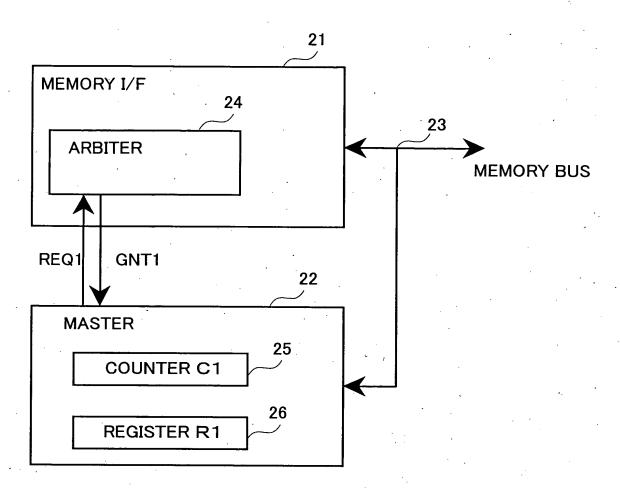
FIG.5





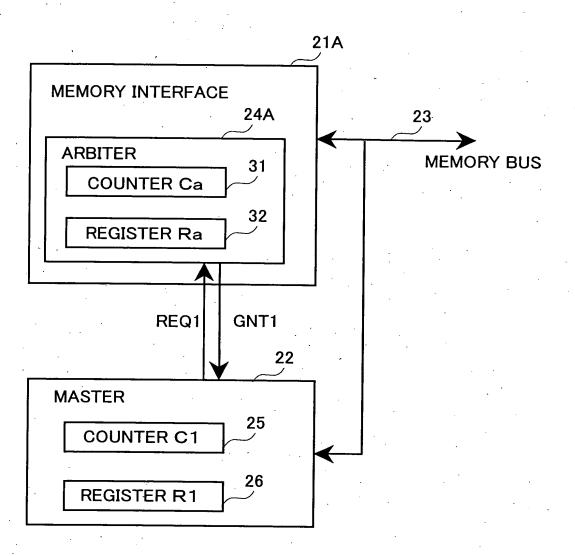
Title: AVOIDANCE OF EXTENDED BUS OCCUPANCY THROUGH SIMPLE CONTROL OPERATION Inventor's Name: ENDO, et al. Application No.: NEW Docket No.: 10035300180

FIG.7



Title: AVOIDANCE OF EXTENDED BUS OCCUPANCY THROUGH SIMPLE CONTROL OPERATION

FIG.8



Title: AVOIDANCE OF EXTENDED BUS OCCUPANCY THROUGH SIMPLE CONTROL OPERATION Inventor's Name: ENDO, et al. Application No.: NEW Docket No.: 10035300180 ACCEPTING REQ1 ACCEPTING REQ1 CLOOK PLOOK REQ1 — GNT1 -COUNTER 25 _ COUNTER 31 '

Title: AVOIDANCE OF EXTENDED BUS OCCUPANCY THROUGH SIMPLE CONTROL OPERATION Inventor's Name: ENDO, et al. Application No.: NEW Docket No.: 10035300180 SDRAM SRAM 2 LCD CONTROL CIRCUIT 26 31 32 GNT1 MEMORY INTERFACE REGISTER Ra COUNTER Ca REQ1 COUNTER REGISTER **ARBITER**

5 GRAPHIC CONTROLLER CPU Θ SYSTEM LSI